

Applicant : Jun Koyama  
Serial No. : 09/912,596  
Filed : July 26, 2001  
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Attorney's Document No.: 12732-056001 / US5129

Amendments to the Drawings:

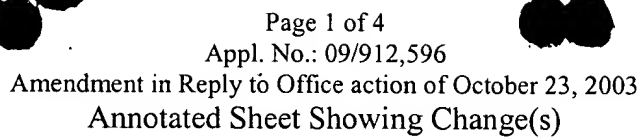
The attached replacement sheets of drawings includes changes to Figs. 13, 14, 19A, 19B, 20A, 20B, 20C, and 20D and replaces the original sheets including Fig. Figs. 13, 14, 19A, 19B, 20A, 20B, 20C, and 20D.

In Figs. 13, 14, 19A, 19B, 20A, 20B, 20C, and 20D, add the legend "Prior Art".

Attachments following last page of this Amendment:

Replacement Sheet (4 pages)

Annotated Sheet Showing Change(s) ( 4 pages)



The diagram shows a source signal line driver circuit 1301, which is a dashed box containing three main blocks: a shift register circuit 1303, a first latch circuit 1304, and a second latch circuit 1305. The shift register circuit 1303 receives S-CLK and S-SP signals and outputs Digital Data. The first latch circuit 1304 receives Digital Data and outputs a Latch Pulse. The second latch circuit 1305 receives the Latch Pulse and outputs G-CLK and G-SP signals. The circuit is powered by a current supply line 1306 (S-V<sub>DD</sub>) and a gate signal line driver circuit 1302. The gate signal line driver circuit 1302 is shown at the top and bottom of the diagram, connected to the G-CLK and G-SP signals. The pixel portion 1307 is shown on the right, connected to the G-CLK and G-SP signals.



Fig. 14  
Prior Art

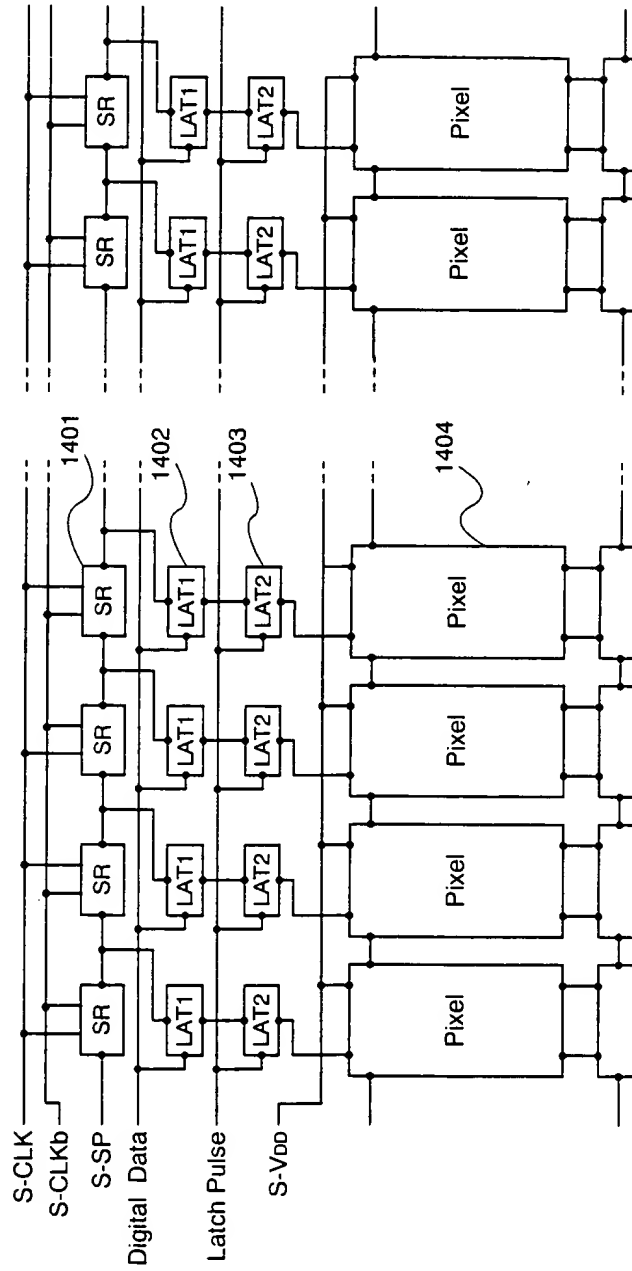




Fig. 19A  
Prior Art

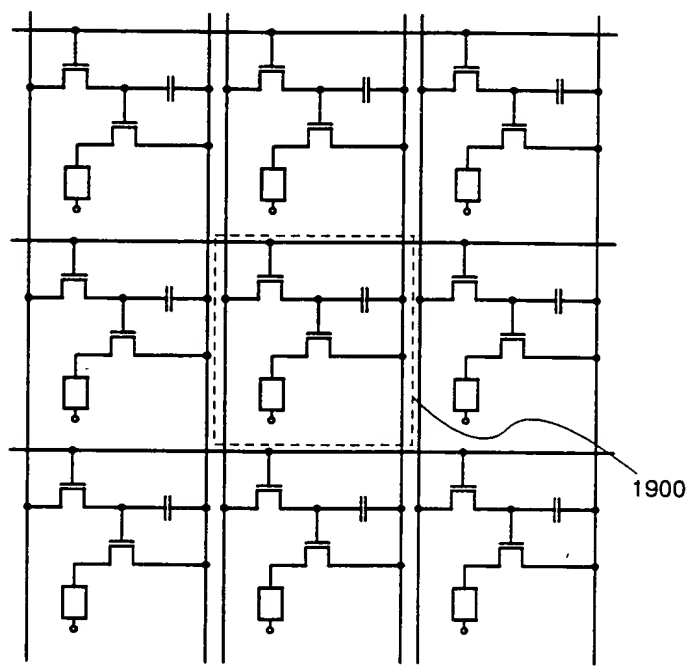


Fig. 19B  
Prior Art

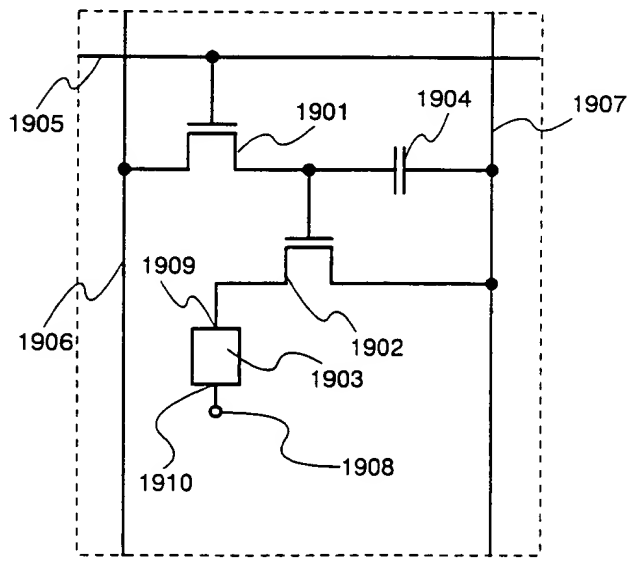




Fig. 20A

Prior Art

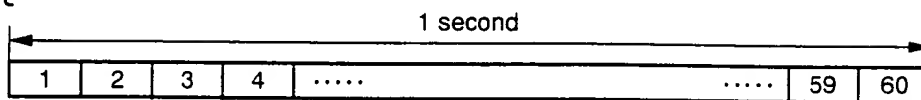


Fig. 20B

Prior Art

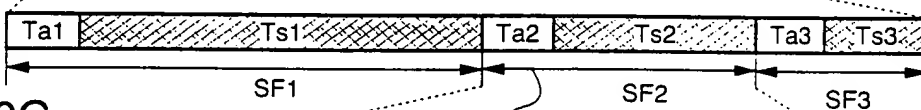


Fig. 20C

Prior Art

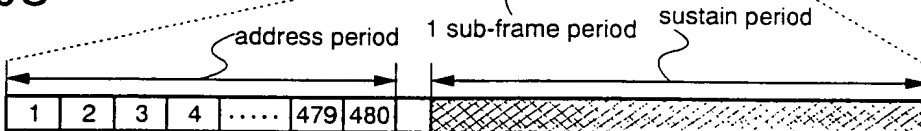


Fig. 20D

Prior Art

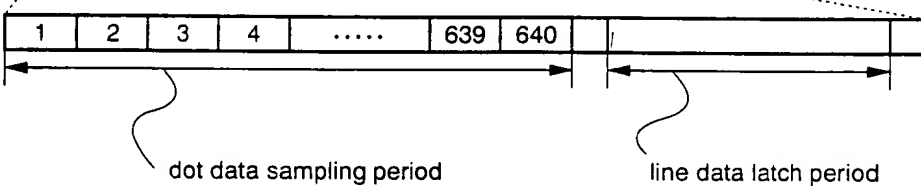




Fig. 13  
Prior Art

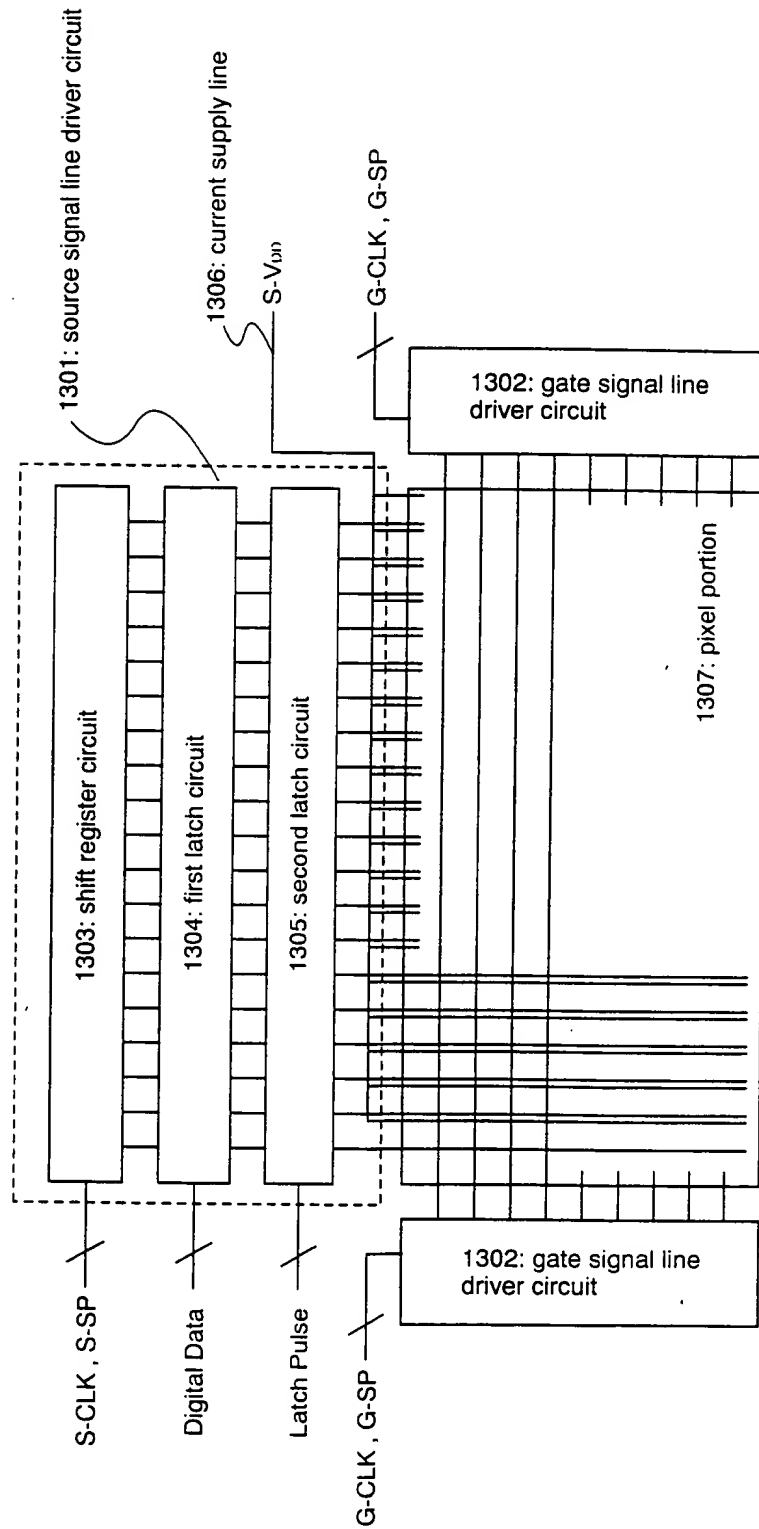




Fig. 14  
Prior Art

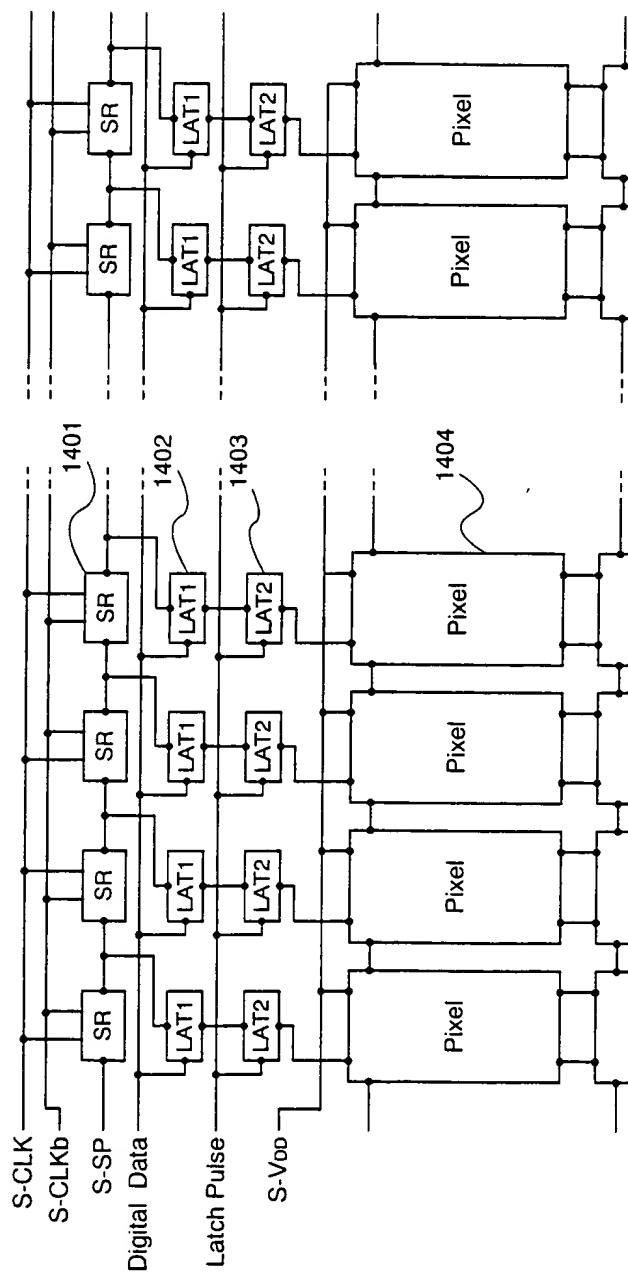




Fig. 19A  
Prior Art

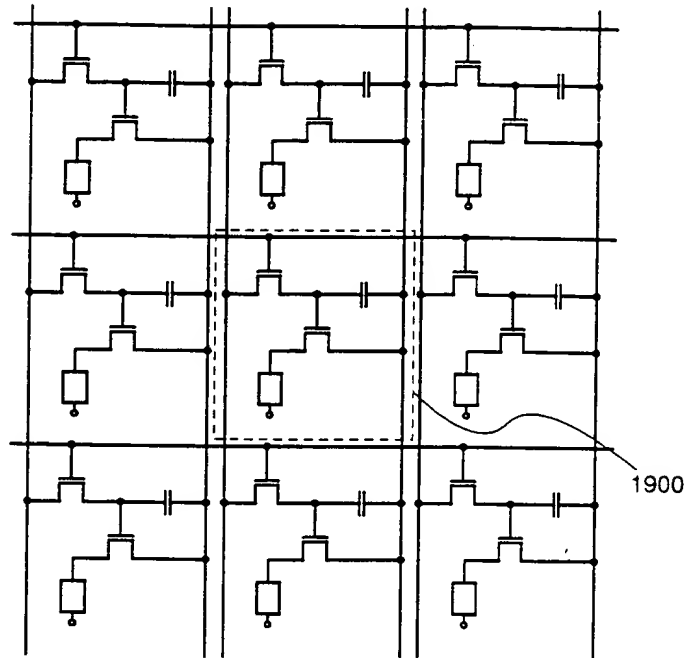


Fig. 19B  
Prior Art

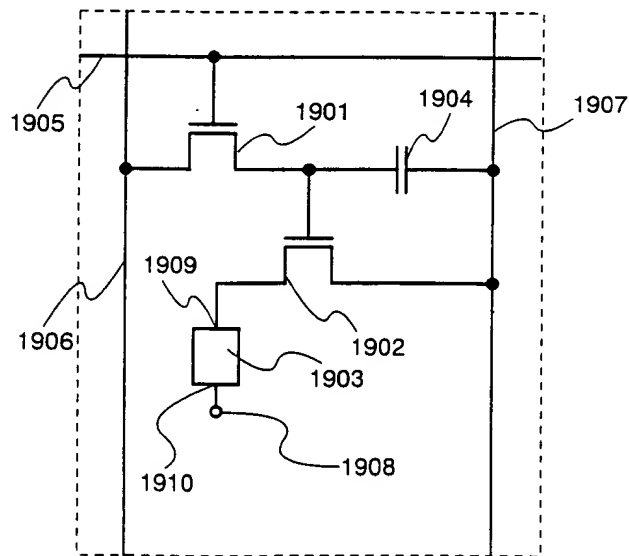






Fig. 20A

Prior Art

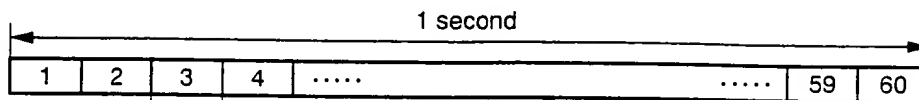


Fig. 20B

Prior Art

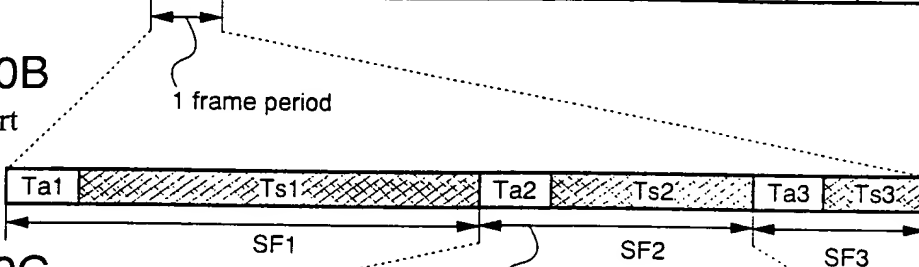


Fig. 20C

Prior Art

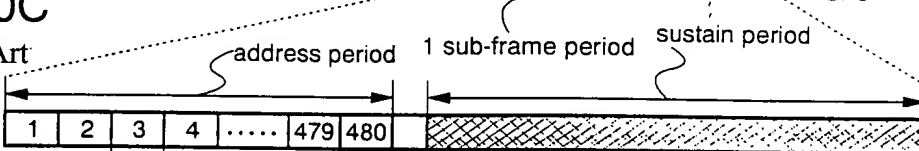


Fig. 20D

Prior Art

